WHAT IS CLAIMED IS:

1. For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a balancing circuit, comprising:

a sensing subcircuit configured to provide a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit configured to generate a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

2. The balancing circuit as recited in Claim 1 wherein said first driver comprises a plurality of vertical PNP transistors.

3. The balancing circuit as recited in Claim 1 wherein said second driver comprises a plurality of vertical NPN transistors.

4. The balancing circuit as recited in Claim 1 wherein said sensing subcircuit comprises at least one diode-connected transistor configured to substantially replicate said current gain characteristic of said first driver.

5. The balancing circuit as recited in Claim 1 wherein said compensation subcircuit comprises a current repeater.

6. The balancing circuit as recited in Claim 1 wherein said compensation subcircuit comprises emitter coupled logic configured to provide said current gain compensation signal.

7. The balancing circuit as recited in Claim 1 wherein said first and second current gain characteristics comprise a ratio of collector-to-base current of devices associated with said first and second drivers.

8. For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a method of operating a balancing circuit, comprising:

providing a correction signal indicating a first current gain characteristic of said first driver; and

generating a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

9. The method as recited in Claim 8 wherein said first driver comprises a plurality of vertical PNP transistors.

10. The method as recited in Claim 8 wherein said second driver comprises a plurality of vertical NPN transistors.

11. The method as recited in Claim 8 wherein said providing is performed by a sensing subcircuit including at least one diode-connected transistor that substantially replicates said current gain characteristic of said first driver.

12. The method as recited in Claim 8 wherein said generating is performed by a compensation subcircuit including a current repeater.

13. The method as recited in Claim 8 wherein said generating is performed by a compensation subcircuit including emitter coupled logic that provides said current gain compensation signal.

14. The method as recited in Claim 8 wherein said first and second current gain characteristics comprise a ratio of collector-to-base current of devices associated with said first and second drivers.

15. A phase locked loop (PLL) circuit, comprising:

a voltage controlled oscillator, coupled to a filter circuit, that receives a signal associated with a charging signal and provides an output signal having an output frequency;

a comparator circuit that provides a comparison signal proportional to a phase difference between said output signal having said output frequency and an input reference signal having an input frequency; and

a charge pump that provides said charging signal via first and second complementary drivers exhibiting different current gain characteristics, said charge pump employing a balancing circuit, including:

a sensing subcircuit that provides a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit that generates a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

16. The PLL circuit as recited in Claim 15 wherein said first driver comprises a plurality of vertical PNP transistors.

17. The PLL circuit as recited in Claim 15 wherein said second driver comprises a plurality of vertical NPN transistors.

18. The PLL circuit as recited in Claim 15 wherein said sensing subcircuit comprises at least one diode-connected transistor that substantially replicates said current gain characteristic of said first driver.

19. The PLL circuit as recited in Claim 15 wherein said compensation subcircuit comprises a current repeater.

20. The PLL circuit as recited in Claim 15 wherein said compensation subcircuit comprises emitter coupled logic that provides said current gain compensation signal.

21. The PLL circuit as recited in Claim 15 wherein said first and second current gain characteristics comprise a ratio of collector-to-base current of devices associated with said first and second drivers.